This book carefully details design tools and techniques for realizing low power and energy efficiency in a highly productive design methodology.

Important topics include:

- Microarchitectural techniques to reduce energy per operation
- Power reduction with timing slack from pipelining
- Analysis of the benefits of using multiple supply and threshold voltages
- Placement techniques for multiple supply voltages
- Verification for multiple voltage domains
- Improved algorithms for gate sizing, and assignment of supply and threshold voltages
- Power gating design automation to reduce leakage
- Relationships among statistical timing, power analysis, and parametric yield optimization

Design examples illustrate that these techniques can improve energy efficiency by two to three times.

My Personal Review:
Recently the requirements for my processor design work have shifted from maximizing performance to minimizing power consumption. This new book from the authors of "Closing the Gap between ASIC & Custom" was published at just the right time. It follows a similar format as the previous book, but instead discusses the considerations involved in minimizing power consumption of processors. The authors again draw extensively on real-world chip design examples and have included contributions from a range of industry experts.

This is a book for chip designers and processor architects. It covers the contribution of and techniques to minimize power consumption from the major factors in processors of leakage, active switching, and clock tree. The book does not discuss the design of software or system hardware outside of processor chips such as batteries, displays, or transceivers.

As academics, the authors have insight into many leading edge design techniques and many companies' commercial chip designs. I know of no other book on low power design that is as deep or thorough a treatment of the subject as this one.

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